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HP E2414B

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HP E2414B Motorola MC68302 Preprocessor Interface User's Guide

for the HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A/62A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, and HP 16550A Logic Analyzers

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Contents

Appendix A: Troubleshooting

Introduction

This user's guide includes information on using the HP E2414B Preprocessor Interface to do logic analysis on the MC68302 microprocessor. The HP E2414B Preprocessor Interface provides a complete interface between any Motorola MC68302 target system and the following logic analyzers: HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A/62A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, and HP 16550A.

Since there is no active circuitry between the microprocessor and the logic analyzer to add skew to signals, the preprocessor interface can be used for timing analysis as well as state analysis.

The HP E2414B configuration software on the flexible disk sets up the format specification menu of the logic analyzer for compatibility with the MC68302 microprocessor. It also loads the inverse assembler for obtaining displays of microprocessor data in the assembly language mnemonics of the microprocessor.

Logic Analyzers Supported

The following logic analyzers are supported by the HP E2414B Preprocessor Interface:

HP 1650A

This logic analyzer provides 1 k of memory depth with either 80 channels of 25 MHz state analysis or 80 channels of 100 MHz timing analysis. The HP 1650A Logic Analyzer requires HP 1650A system software version V1.11 or higher to operate with the HP E2414B Preprocessor Interface. If your HP 1650A software version is older than V1.11, load new HP 1650A software (V1.11 or higher) before loading the HP E2414B software.

HP 1650B, HP 1652B, HP 16510A, and HP 16510B

These logic analyzers provide 1 k of memory depth with either 80 channels of 35 MHz state analysis (25 MHz state analysis for the HP 16510A) or 80 channels of 100 MHz timing analysis.

HP 16511B

This logic analyzer combination provides 1 k of memory depth with either 160 channels of 35 MHz state analysis, or 80 channels of 35 MHz state analysis and 80 channels of 100 MHz timing analysis.

HP 1660A/61A/62A

The HP 1660A/61A/62A Logic Analyzers provide 4 k of memory depth with 136 channels (HP 1660A), 102 channels (HP 1661A), or 68 channels (HP 1662A) of 100 MHz state analysis or 250 MHz timing analysis. These logic analyzers also support various combinations of mixed state/timing analysis.

HP 16540A,D with one or two HP 16541A,D Expansion Cards

This logic analyzer combination provides 4 k of memory depth (16 k with the D version) with up to either 64 or 112 channels of 100 MHz state or timing analysis.

HP 16542A (Master Card and two expansion cards)

This logic analyzer combination provides 1 M of memory depth with 48 channels of 100 MHz state or timing analysis.

HP 16550A

This logic analyzer provides 4 k of memory depth with 102 channels per card of 100 MHz state analysis or 250 MHz timing analysis. The logic analyzer will also support various combinations of mixed state/timing analysis.

How to Use This Manual

This manual is organized into three chapters and one appendix:

- Chapter 1 explains how to install and configure the HP E2414B Preprocessor Interface to perform measurements with the supported logic analyzers.
- Chapter 2 provides reference information on the format specification and symbols configured by the HP E2414B software. It also provides information about the inverse assembler and status encoding.
- Chapter 3 contains additional reference information including the characteristics and signal mapping for the HP E2414B Preprocessor Interface.
- Appendix A contains information on troubleshooting problems or difficulties which may occur with the preprocessor interface.

1

Setting Up the HP E2414B

Introduction

This chapter explains how to install and configure the HP E2414B Preprocessor Interface to perform measurements with the supported logic analyzers.

Duplicating the Master Disk

Before you use the HP E2414B software, make a duplicate copy of the HP E2414B master disk. Then store the master disk and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the disk wears out, is damaged, or a file is accidently deleted.

To make a duplicate copy, use the Duplicate Disk operation in the disk menu of your logic analyzer. For more information, refer to the reference manual for your logic analyzer.

Equipment Supplied

The HP E2414B Preprocessor Interface consists of the following equipment:

- The preprocessor interface hardware, which includes the preprocessor interface circuit card.
- The configuration files and inverse assembler software on a 3.5-inch disk.
- This user's guide.

Note

The preprocessor interface socket assembly pins are covered at the time of shipment with a protective foam pad. This is done to protect the delicate gold plated pins of the assembly from damage due to impact. When you're not using the preprocessor interface, protect the socket assembly pins from damage by covering them with the foam protector.

Minimum Equipment Required

The minimum equipment required for analysis of MC68302 target systems consists of the following items:

- An HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A/62A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D (Master Card and one or two expansion cards), HP 16542A (Master Card and two expansion cards), or HP 16550A Logic Analyzer. The HP 1650A Logic Analyzer requires HP 1650A system software version V1.11 or higher to operate with the HP E2414B.
- The HP E2414B Preprocessor Interface.
- HP E2414B option 1CC for MC68302 QFP microprocessors.

Note

The above equipment is the minimum required for three-pod state analysis. There are six additional connectors on the preprocessor interface which can be used for timing analysis; however, the six additional connectors require either the General Purpose Probes shipped with your logic analyzer, or one 100 kOhm Termination Adapter per connector (HP part number 01650-63203).

Installation Overview

The following procedure describes the major steps required to perform measurements with the HP E2414B Preprocessor Interface. The page numbers listed in the various steps refer you to sections in this manual that offer more detailed information.

Caution 

To prevent equipment damage, be sure to remove power from both the logic analyzer and the target system whenever the preprocessor interface is being connected or disconnected.

1. Install the preprocessor interface on the target system (see page 1-4).
2. Plug the logic analyzer pods into the preprocessor interface as shown in table 1-1 (see pages 1-8 and 1-9). The 2 x 20-pin wide connectors do not require termination adapters. For pods P2, P5 and P6, connect 100 kOhm Termination Adapters (see page 1-10).
3. Load the logic analyzer configuration and inverse assembler by loading the appropriate file from the disk (see page 1-11).

You are now ready to make measurements with the logic analyzer. The rest of this chapter contains more detailed information on setting up the hardware and software.

Connecting to the Target System

The HP E2414B Preprocessor Interface can be used with PGA or QFP target systems. QFP target systems require HP E2414B option 1CC, which includes the *QFP Probe Adapter Assembly Operating Note*. For QFP target systems, use the instructions in the *QFP Probe Adapter Assembly Operating Note*. For PGA target systems, use the following steps to connect the preprocessor interface to your target system:

Caution 

To prevent equipment damage, be sure to remove power from both the logic analyzer and the target system whenever the preprocessor interface is being connected or disconnected.

1. Remove the MC68302 microprocessor from its socket on the target system and store it in a protected environment.

Caution 

Serious damage to the target system or preprocessor interface can result from incorrect connection. Note the position of pin A1 (figure 1-1) on the preprocessor interface connector and the target system socket prior to making connections. Also, take care to align the connectors so that all pins are making contact.

2. Plug the preprocessor interface into the microprocessor socket on the target system, noting the position of pin A1 (see figure 1-1). There is a notch on the socket indicating pin A1.

Note 

If the preprocessor interface connector interferes with components of the target system, or if a higher profile is required, additional plastic pin guards can be added. Plastic pin guards can be ordered from Hewlett-Packard using the part number 1200-1679. However, any 132-pin PGA IC socket with an MC68302 footprint and gold-plated pins can be used.

3. Plug the MC68302 microprocessor into the socket on the preprocessor interface, again ensuring that the A1 pins are aligned. The socket is designed with low-insertion-force pins to allow you to install or remove the microprocessor with minimum force.

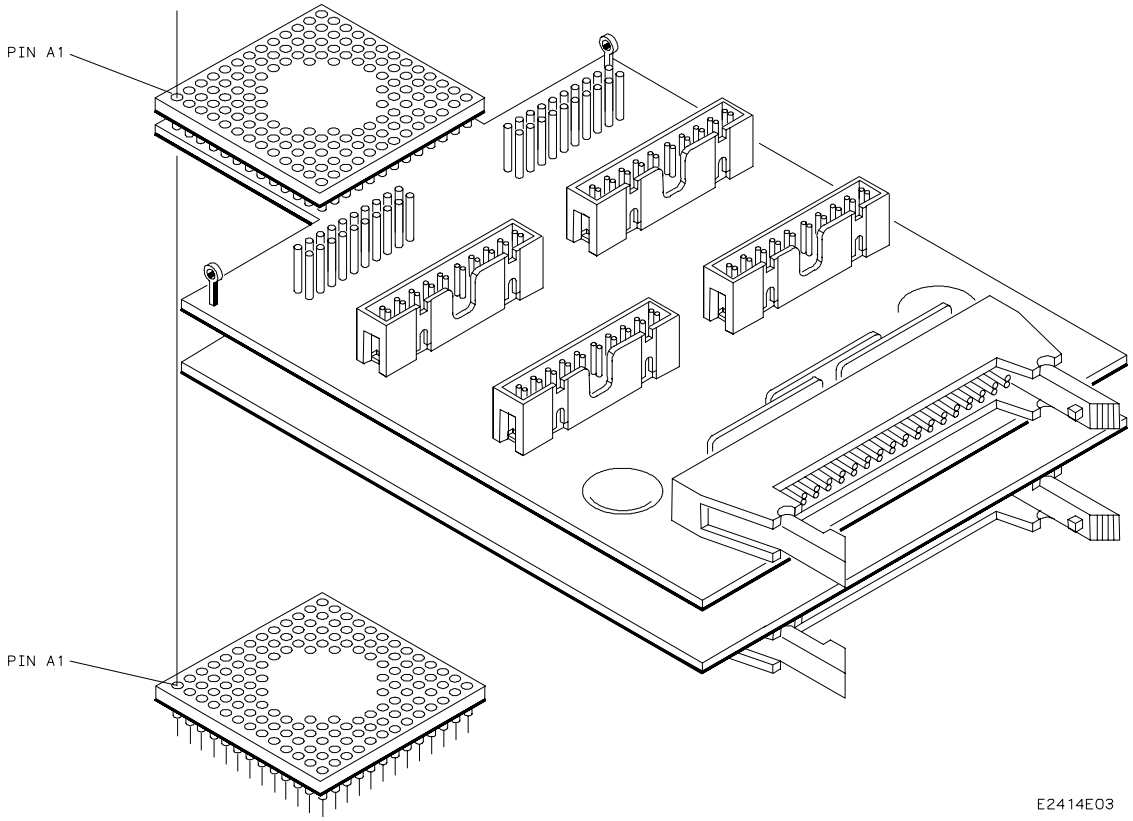

Figure 1-1. HP E2414B Preprocessor Interface

Caution Care must be used when removing a microprocessor from the preprocessor interface board to prevent damaging the circuit traces.

Connecting to the HP E2414B

Connect the logic analyzer cables to the preprocessor interface as shown in table 1-1 (pages 1-8 and 1-9). Designations such as P1 refer to connectors on the preprocessor interface, while Pod 1 refers to a logic analyzer pod.

Figure 1-2 shows the relative locations for the logic analyzer cards.

Note

HP 16542A with three or four Expansion Cards

The locations for the HP 16542A expansion cards, relative to the Master Card, depend on the number of expansion cards used. If two expansion cards are used, one is located above the Master Card and one is located below the Master Card. If three expansion cards are used, two of them are located above the Master Card and the third is located below the Master Card. When four expansion cards are used, they are located as shown in figure 1-2.

Table 1-1 shows the physical location and connections for a two-expansion-card system. If you are using more than two expansion cards, and want to connect additional pods, check the Format menu in the logic analyzer to see where the pods should be connected.

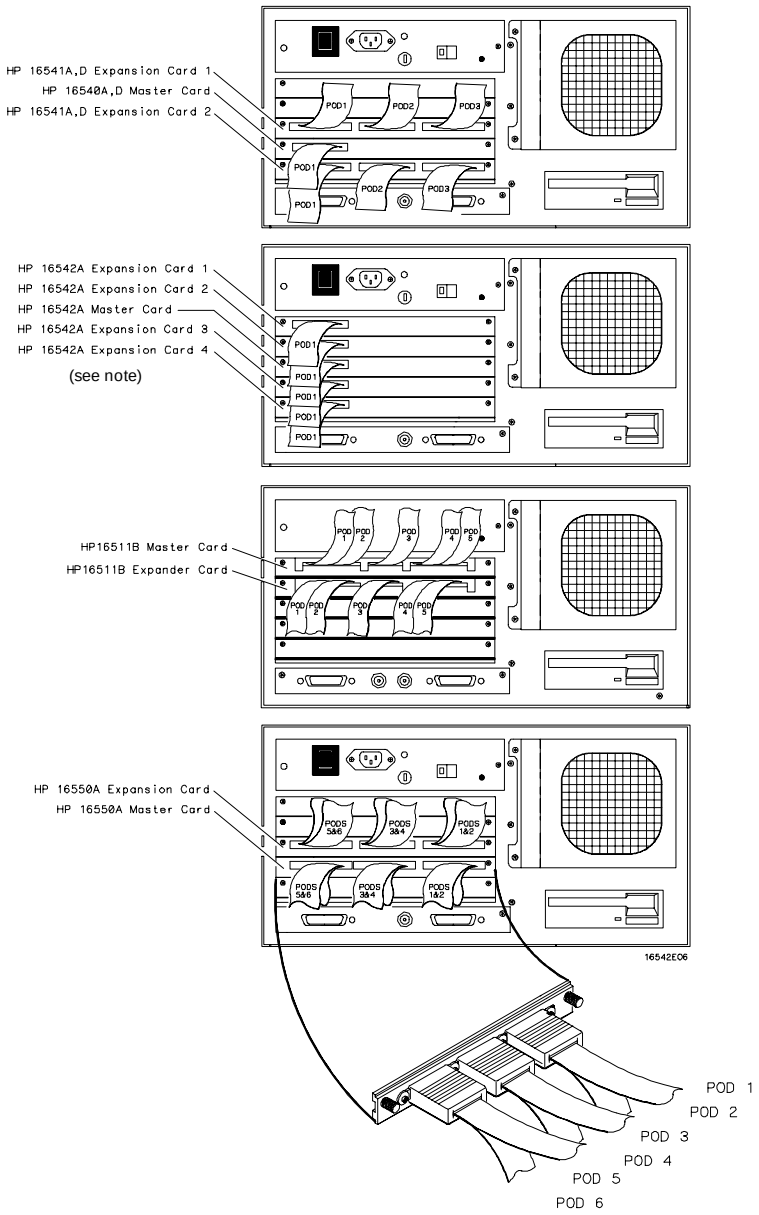

Figure 1-2. Logic Analyzer Card Locations
(relative locations, actual slots used may vary)

Table 1-1. Logic Analyzer Connections and Configuration Files (HP 1650 series, HP 16510A/B, HP 16511B, HP 16540/16541A,D, HP 16550A)

Logic Analyzer	File	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 1650A/B, HP 1652B, HP 16510A/B	C68302		*	** P4 ADDR/ STAT	P3 ADDR	*	P1 DATA clk ↑
HP 16511B Upper Card	D68302		--	--	--	--	--
HP 16511B Lower Card			*	** P4 ADDR/ STAT	P3 ADDR	*	P1 DATA clk ↑
HP 16541A,D Exp. Card 1	E68302				*	** P4 ADDR/ STAT	P3 ADDR
HP 16540A,D Master Card							P1 DATA clk ↑
HP 16541A,D Exp. Card 1	E68302_6				--	P6	P2
HP 16540A,D Master Card							P1 DATA clk ↑
HP 16541A,D Exp. Card 2					P5	** P4 ADDR/ STAT	P3 ADDR
HP 16550A	F68302	*	** P4 ADDR/ STAT	*	P3 ADDR	*	P1 DATA clk ↑

* P2, P5, and P6 on the preprocessor interface are not required for inverse assembly. They can be connected to any logic analyzer pod marked with an asterisk (*), or left unconnected at the user's discretion. Use GP Probes or termination adapters to monitor these signals (see next section).

** For state analysis and inverse assembly, only the terminated (2 x 20-pin wide) P4 connector can be used. For timing analysis either the terminated or nonterminated P4 connector can be used.

Table 1-1. Logic Analyzer Connections and Configuration Files (HP 16542A, HP 1660 series)

Logic Analyzer	File	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 16542A Exp. Card 1	E68302						** P4 ADDR/ STAT
HP 16542A Master Card							P1 DATA clk ↑
HP 16542A Exp. Card 2							P3 ADDR
HP 1660A/ 61A/62A	C68302	*	*	*	P1 DATA clk ↑	** P4 ADDR/ STAT	P3 ADDR
HP 1660A	F68302	**(Pod 7)** ** P4 ADDR/ STAT	*	*	P3 ADDR	*	P1 DATA clk ↑
HP 1661A		*	** P4 ADDR/ STAT	*	P3 ADDR	*	P1 DATA clk ↑
HP 1662A				*	** P4 ADDR/ STAT	P3 ADDR	P1 DATA clk ↑
HP 1660A	E68302_6	**(Pod 8)** P6	**(Pod 7)** P2	P5	P1 DATA clk ↑	** P4 ADDR/ STAT	P3 ADDR
HP 1661A		P6	P2	P5	P1 DATA clk ↑	** P4 ADDR/ STAT	P3 ADDR
HP 1662A				P5	P1 DATA clk ↑	** P4 ADDR/ STAT	P3 ADDR

Connecting the Termination Adapters

The logic analyzer probes must be properly terminated for the logic analyzer to operate correctly. On the preprocessor interface, there are nine connectors. P1, P3, and P4 have both terminated and nonterminated connectors, while P2, P5, and P6 only have nonterminated connectors. You can probe P2, P5, and P6 (and the nonterminated P1, P3, and P4 connectors) with the General Purpose Probes shipped with your logic analyzer or by using 100 kOhm Termination Adapters (HP part number 01650-63203). The following steps explain how to connect the termination adapters to the preprocessor interface:

1. Align the key on the male end of the termination adapter with the slot on the connector of one of the logic analyzer cables, and push the termination adapter into the connector.
2. Connect the female end of the termination adapter to the preprocessor interface.
3. Repeat steps 1 and 2 for each termination adapter.

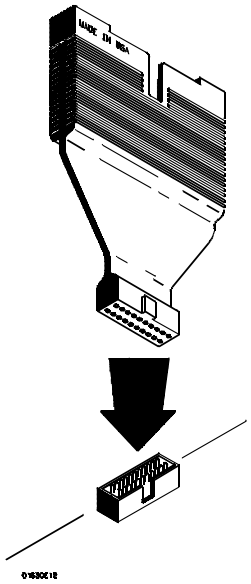

Figure 1-3. Connecting the Termination Adapter

Setting Up the Analyzer from the Disk

The logic analyzer is configured for state analysis by loading the appropriate configuration file. Loading this file also loads the inverse assembler. To load the configuration and inverse assembler:

1. For the HP 1650A Logic Analyzer, ensure that the HP 1650A system software version is V1.11 or higher.
2. Install the HP E2414B disk in the front disk drive of the logic analyzer.
3. Select one of the following menus:
   - For the HP 1650-series logic analyzers, select the I/O Disk Operations menu;
   - For the HP 16500-series and HP 1660-series logic analyzers, select the System Front Disk menu.
4. Configure the menu to "Load" the analyzer configuration from disk.
5. For HP 16500-series and HP 1660-series logic analyzers, select the appropriate module (such as "100/500 MHz LA" or "Analyzer") for the load.
6. Use the knob to select the appropriate configuration file (see table 1-1).
7. Execute the load operation to load the file into the logic analyzer.

Timing Analysis

The HP E2414B can also be used for timing analysis. The format specification loaded for state analysis is used for timing analysis. To configure the logic analyzer for timing analysis:

1. Load the appropriate state configuration file from the disk.
2. Select the Configuration menu of the logic analyzer.
3. Select the Type field and select Timing.

Probing With an Oscilloscope

The individual pins on the preprocessor interface can also be probed with an oscilloscope. There are two ground pins on the top of the preprocessor interface (see figure 1-4). Connect the ground lead of the oscilloscope to one of the ground pins on the preprocessor interface, and the other lead to the signal to be measured. For QFP target systems, you can probe the signals at the PGA socket. For PGA target systems, the signals are available on the six nonterminated pods (see top of figure 1-4). Table 3-1 in Chapter 3 lists the correlation between the microprocessor signals, the PGA socket, and the connectors.

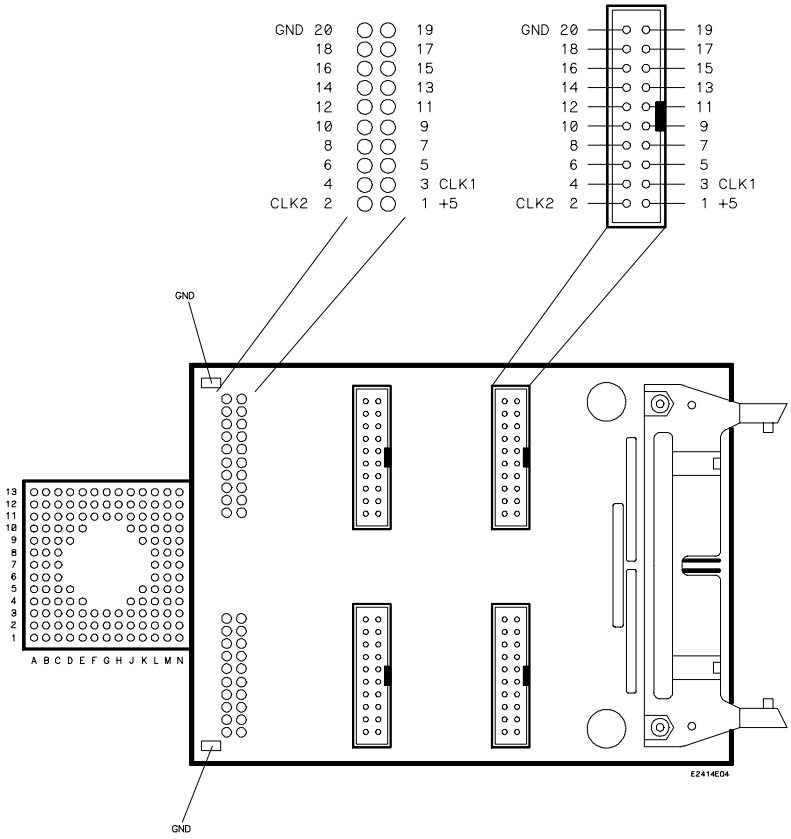

Figure 1-4. Pin Numbers and Ground Pins

2

Analyzing the MC68302

Introduction

This chapter provides reference information on the format specifications and symbols configured by the HP E2414B software. It also provides information about the inverse assembler and status encoding.

Format Specification

The format specification for the logic analyzer is set up by the HP E2414B software similar to that shown in figure 2-1. There will be some slight differences in the displays, according to which logic analyzer you are using. For example, some logic analyzers do not have a Clock Period field.

The label DATA_B is included in the format specification to give you a convenient method of displaying the microprocessor data in both hexadecimal and mnemonic formats. This field makes it easier to specify a trace specification from the data in the listing menu.

Chapter 3 lists the microprocessor signals for the HP E2414B and their corresponding lines to the logic analyzer.

Note 

For those logic analyzers which have a Clock Period field (HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, and HP 16511B), the Clock Period field should remain in the current selection (> 60 ns) for proper HP E2414B operation. For more information on the Clock Period field, refer to the reference manual for your logic analyzer.

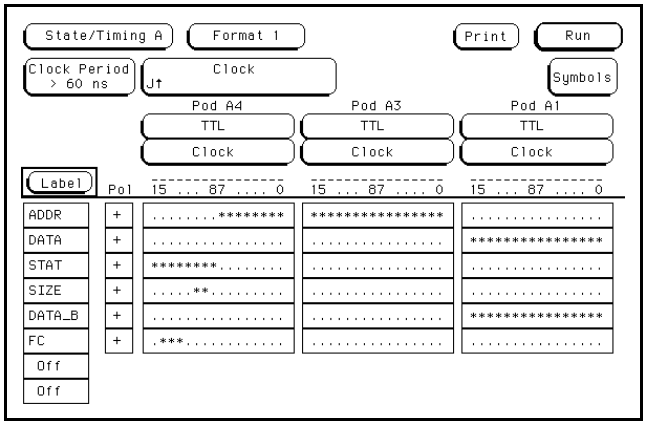

Figure 2-1. 68302 Format Specification

Symbols

The configuration files set up symbol tables on the logic analyzer. The tables contain alphanumeric values which identify data patterns or ranges. Table 2-1 lists a description of the bits in the STAT label. Table 2-2 lists the STAT Field Encoding. Table 2-3 lists the Symbols.

Table 2-1. STAT Label Bits

Bit	Status Signals	Description
0	R/W	This signal is high for read cycles and low for write cycles.
1	LDS	This signal functions as the lower data strobe for 16-bit data busses and as the data strobe for 8-bit busses.
2	UDS/A0	This signal functions as the upper data strobe for 16-bit data busses and as A0 for 8-bit busses.
3	--	On the terminated P4 connector this signal is tied high at all times. It is not connected to the nonterminated P4 connector.
4 - 6	FC0 - FC2	These signals indicate the type of cycle the microprocessor is executing.
7	BGACK	This signal is low when the microprocessor has granted control of the bus to another device.

Table 2-2. STAT Field Encoding

Microprocessor Cycle Type	STAT Bit 7 6 5 4 3 2 1 0
Bus Grant	0 x x x x x x x
User Data Write	1 0 0 1 x x x 0
User Data Read	1 0 0 1 x x x 1
User Program Read	1 0 1 0 x x x 1
Supervisor Data Write	1 1 0 1 x x x 0
Supervisor Data Read	1 1 0 1 x x x 1
Supervisor Program Read	1 1 1 0 x x x 1
Interrupt Acknowledge	1 1 1 1 x x x x
Size of Transfer	
Low Byte Transfer	x x x x x 1 0 x
High Byte Transfer	x x x x x 0 1 x
Word Transfer	x x x x x 0 0 x

Table 2-3. MC68302 Symbols

Label	Symbol	Pattern
STAT	DMA	0xxx xxxx
	USER DATA WRITE	1001 xxx0
	USER DATA READ	1001 xxx1
	USER PRGM READ	1010 xxx1
	SUPR DATA WRITE	1101 xxx0
	SUPR DATA READ	1101 xxx1
	SUPR PRGM READ	1110 xxx1
	INTERRUPT ACK	1111 xxxx
	OPCODE FETCH	1x10 xxx1
	READ	xxxx xxx1
	WRITE	xxxx xxx0
SIZE	LOW BYTE	10
	HIGH BYTE	01
	WORD	00
FC	USER DATA	001
	USER PRGM	010
	SUPR DATA	101
	SUPR PRGM	110
	INTR ACK	111
	USER	0xx
	SUPR	1xx
	DATA	x01
	PRGM	x10

Listing Menu

Captured data is displayed as shown below. These figures display the state listing for 16-bit bus cycles. The inverse assembler is constructed so the mnemonic output closely resembles the actual assembly source code.

The logic analyzer always probes the full 16-bit data bus of the microprocessor. There are some instructions that use only 8 bits for memory transactions. When fewer than the full 16 bits of the data bus are used by a memory cycle, the inverse assembler marks the bits not used by the microprocessor with an "x."

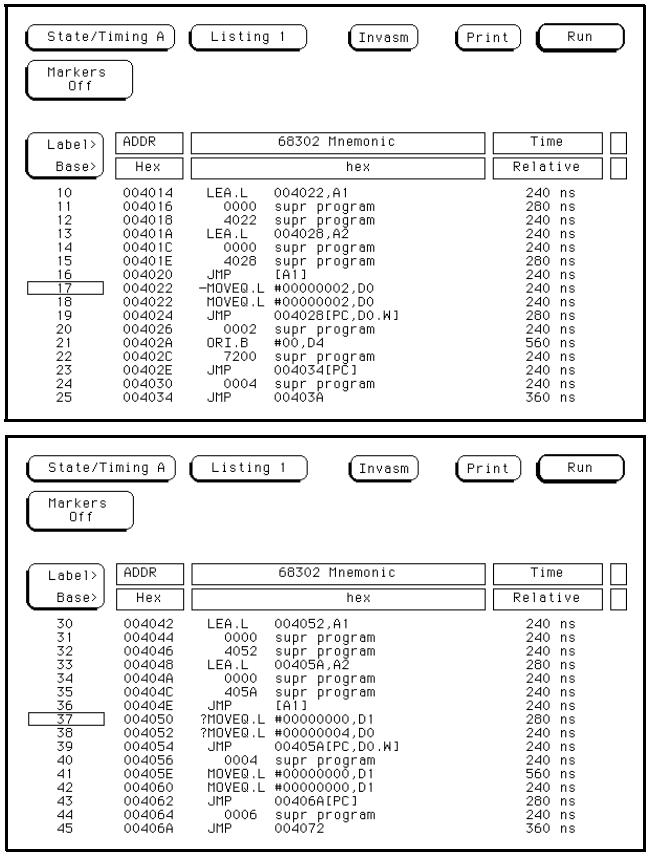

Figure 2-2. State Listings

The Inverse Assembler

The inverse assembler determines whether the MC68302 is operating in 8-bit or 16-bit mode, and disassembles the code accordingly.

The microprocessor does not provide enough status information for the inverse assembler to pick out the first word of an opcode fetch from a series of program reads. For correct disassembly, you must point to the 16-bit word that contains the first word of an opcode fetch. Once synchronized, the inverse assembler disassembles from this point through the last line of the display. To point to the first word of an opcode fetch:

1. Select a line on the display that you know contains the first word of an instruction fetch.
2. Roll this line to the top of the display.

Note 

The cursor location is not the top of the display. In figure 2-2, lines 10 and 30 are at the top of the displays.

---

3. Select the "Invasm" field at the top of the display. The listing inverse assembles from the top line down. Any data before this display is left unchanged.

Rolling the display up inverse assembles the lines as they appear on the bottom of the display. If you jump to another area of the display by entering a new line number, you may have to re-synchronize the inverse assembler by repeating steps 1 through 3.

Note 

Each time you inverse assemble a block of memory, the analyzer keeps that block in the inverse assembled condition. You can inverse assemble several different blocks in the analyzer memory, but the activity between those blocks will not be inverse assembled.

Interpreting Data

In general, asterisks indicate that expected operand fetches are not stored in the logic analyzer memory. A pair of asterisks (**) displayed in the operand field of an instruction indicates that a byte of an expected operand was not stored in the logic analyzer memory. Four asterisks (****) indicate that one word of an expected operand was missing. Missing operands (or parts of operands) can result from microprocessor instruction prefetch activity or storage qualification.

Examples:

```
ORI.B    # **,D2          (missing byte operand)
ORI.W    # ****,D1        (missing word operand)
ORI.L    # 234A****,D3    (missing lower word of the operand)
ORI.L    # ********,D3    (missing both words of the operand)
```

The microprocessor is capable of supporting byte, word, and long word (32-bit) operands. During operand reads and writes, entire 16-bit (word) values appear on the microprocessor data bus. In the case of single-byte operands, the inverse assembler displays "xx" for the byte of the input data that is ignored by the microprocessor. In this manner, you can determine exactly which byte of data the microprocessor has used as an operand.

Examples:

```
ORI.B    # 03,D1          xx03 program read     (microprocessor uses
                                                lower byte only)
ORI.W    # 1203,D1        1203 program read     (microprocessor uses
                                                both bytes of the word)
```

PC-based Addressing Modes

The 68302 microprocessor may occasionally make an operand fetch from program space when program counter (PC) -based addressing modes are used. For example:

```
MOVE.L 0[PC,D0.L],D7
```

When this occurs, the resulting memory read is classified as a program reference by the 68302, and the Function Code lines driven accordingly (they indicate a program read rather than a data read).

When the inverse assembler detects an instruction of this sort, it will attempt to locate the operand fetch and tag it so that it will not be disassembled. Instead, it will be classified as "program data" by the inverse assembler, and displayed in hex.

Table 2-4 shows an example. State 350 has the instruction, and states 355 and 356 have the data.

Table 2-4. PC-based Addressing Mode Listing

Label Base	> ADDR > Hex	DATA Invasm	STAT Symbol
348	04D214	MOVE.L D7,FFCE[A4]	USER PGRM READ
349	04D216	FFCE user program read	USER PGRM READ
350	04D218	MOVE.L 04D654[PC],-[A7]	USER PGRM READ
351	F4083E	43D8 user data write	USER DATA READ
352	F40840	6DFB user data write	USER DATA READ
353	04D21A	043A user program read	USER PGRM READ
354	04D21C	MOVE.L D7,-[A7]	USER PGRM READ
355	04D654	4400 user program data	USER PGRM READ
356	04D656	0000 user program data	USER PGRM READ
357	04D21E	JSR 03523C	USER PGRM READ
358	086BBC	0000 user data write	USER DATA READ
359	086BBA	4400 user data write	USER DATA READ
360	04D220	0003 user program read	USER PGRM READ
361	086BB8	6DFB user data write	USER DATA READ
362	086BB6	43D8 user data write	USER DATA READ
363	04D222	523C user program read	USER PGRM READ

Unused Prefetches (– / ?)

The microprocessor may fetch up to two instruction words while the last opcode is still being executed. When a program executes an instruction that causes a branch, prefetched words are not used and are discarded by the microprocessor. Unused prefetches are indicated by the prefix "–" in the inverse assembly listing as shown in line 17 of figure 2-2 (top) on page 2-5.

The logic analyzer captures prefetches, even if they are not executed. Care must be taken if you are specifying a trigger condition or a storage qualification when the instruction of interest follows an instruction that may cause branching. An unused prefetch may generate an unwanted trigger.

Since the microprocessor only prefetches one word, one technique to avoid unwanted triggering from unused prefetches is to add "2" to the trigger address. This trigger condition is only satisfied if the branch is not taken.

In some cases, it is impossible to determine from bus activity whether or not a branch is taken or a prefetch is executed. In these cases, the inverse assembler marks the disassembled line with the prefix "?" as shown in line 37 of figure 2-2 (bottom).

Error Messages

The following list of messages will help you identify operation errors.

Data Error Trace data collected by the logic analyzer cannot be retrieved from memory. Indicates a hardware error or inverse assembler software error.

Illegal Opcode Undefined opcode encountered. Microprocessor action cannot be determined.

Note

Do not modify the bits in the STAT or DATA labels, or the lower bits in the ADDR label in the format specification if you want inverse assembly. Changes may cause incorrect results. Also note that if the trace specification is modified to store only selected bus cycles, incorrect or incomplete inverse assembly may result.

For the above qualification, the lower bits are bits 0 - 15 for the ADDR label. You can modify ADDR bits 16 - 23.

3

General Information

Introduction

This chapter contains the characteristics and signal mapping for the HP E2414B Preprocessor Interface.

HP E2414B Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the HP E2414B Preprocessor Interface. These characteristics are included as additional information for the user.

Product Compatibility: Motorola MC68302 microprocessors, and all microprocessors made by other manufacturers which comply with Motorola MC68302 specifications.

Microprocessor Package: 132-pin PGA.
132-pin QFP (with option 1CC).

Accessories Required: None.

Clock Speed: 20 MHz CLK (10 MHz AS rate).

Note 

On a read cycle, data must be valid for 10 ns before the rising edge of AS for all logic analyzers except the HP 16540/16541A,D, HP 16542A, HP 16550A, and HP 1660 series.

Signal Line Loading: 100 kΩ plus 12 pF on all lines.

Logic Analyzer Required: HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A/62A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D (Master Card and one or two expansion cards), HP 16542A (Master Card and two expansion cards), or HP 16550A.

Number of Probes Used: Up to six 16-channel probes.

Power Requirements: 1 mA at + 5 Vdc maximum from the logic analyzer.

Microprocessor Operations Displayed:	User Data Read/Write User Program Read Supervisor Data Read/Write Supervisor Program Read Interrupt Acknowledge Bus Grant	
Additional Capabilities:	The logic analyzer captures all bus cycles, including prefetches.	
Environmental Temperature:	Operating:	0 to + 55 °C (+ 32 to + 131 °F)
	Nonoperating:	–40 to + 75 °C (–40 to + 167 °F)
Altitude:	Operating:	4,600 m (15,000 ft)
	Nonoperating:	15,300 m (50,000 ft)
Humidity:	Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.	

Clocking

The microprocessor's address strobe (AS) indicates that address, function code, size, and R/W state information is on the bus and valid. The logic analyzer uses the rising edge of AS to clock information into the logic analyzer.

Signal-to-Connector Mapping

The following table describes the electrical interconnections implemented with the HP E2414B Preprocessor Interface. Since the pods on the logic analyzers are numbered differently than the pods on the preprocessor interface, refer to table 1-1 to correlate the pod numbers.

Table 3-1. Signal-to-Connector List

E2414B Connector / Pin	Logic Analyzer Bit	Preprocessor Interface / PGA Pin	QFP Pin	Pin Mnemonic	Label
P3 / 19	0	N5	106	UDS	ADDR
P3 / 18	1	G1	1	A1	ADDR
P3 / 17	2	G3	2	A2	ADDR
P3 / 16	3	G2	3	A3	ADDR
P3 / 15	4	F2	5	A4	ADDR
P3 / 14	5	F3	6	A5	ADDR
P3 / 13	6	E1	7	A6	ADDR
P3 / 12	7	D1	8	A7	ADDR
P3 / 11	8	E2	9	A8	ADDR
P3 / 10	9	E3	10	A9	ADDR
P3 / 9	10	C1	11	A10	ADDR
P3 / 8	11	B1	12	A11	ADDR
P3 / 7	12	D3	14	A12	ADDR
P3 / 6	13	C2	15	A13	ADDR
P3 / 5	14	A1	16	A14	ADDR
P3 / 4	15	D4	17	A15	ADDR
P4 / 19	0	D5	19	A16	ADDR
P4 / 18	1	C3	20	A17	ADDR
P4 / 17	2	B2	21	A18	ADDR
P4 / 16	3	B3	22	A19	ADDR
P4 / 15	4	B4	24	A20	ADDR
P4 / 14	5	A2	25	A21	ADDR
P4 / 13	6	A3	26	A22	ADDR
P4 / 12	7	C5	27	A23	ADDR

Table 3-1. Signal-to-Connector List (Continued)

E2414B Connector / Pin	Logic Analyzer Bit	Preprocessor Interface / PGA Pin	QFP Pin	Pin Mnemonic	Label
P4 / 11	8	N6	103	R/W	STAT
P4 / 10	9	L6	105	LDS	STAT
P4 / 9	10	N5	106	UDS/A0	STAT
P4 / 8	11	--	--	--	STAT
P4 / 7	12	H1	132	FC0	STAT
P4 / 6	13	H3	130	FC1	STAT
P4 / 5	14	J1	129	FC2	STAT
P4 / 4	15	M11	88	BGACK	STAT
P1 / 19	0	B11	48	D0	DATA
P1 / 18	1	C10	47	D1	DATA
P1 / 17	2	B10	46	D2	DATA
P1 / 16	3	A12	45	D3	DATA
P1 / 15	4	C9	43	D4	DATA
P1 / 14	5	B9	42	D5	DATA
P1 / 13	6	A10	41	D6	DATA
P1 / 12	7	A9	40	D7	DATA
P1 / 11	8	B8	38	D8	DATA
P1 / 10	9	A8	37	D9	DATA
P1 / 9	10	B7	36	D10	DATA
P1 / 8	11	C7	35	D11	DATA
P1 / 7	12	A6	33	D12	DATA
P1 / 6	13	B6	32	D13	DATA
P1 / 5	14	C6	31	D14	DATA
P1 / 4	15	A5	30	D15	DATA

Table 3-1. Signal-to-Connector List (Continued)

E2414B Connector / Pin	Logic Analyzer Bit	Preprocessor Interface / PGA Pin	QFP Pin	Pin Mnemonic	Label
P2 / 19	0	K1	128	CS0	(Note 1)
P2 / 18	1	J2	127	CS1	(Note 1)
P2 / 17	2	L1	125	CS2	(Note 1)
P2 / 16	3	M1	124	CS3	(Note 1)
P2 / 15	4	L8	97	IPL0	(Note 1)
P2 / 14	5	N9	96	IPL1	(Note 1)
P2 / 13	6	N10	95	IPL2	(Note 1)
P2 / 12	7	N2	111	TIN1	(Note 1)
P2 / 11	8	L4	113	TOUT1	(Note 1)
P2 / 10	9	M3	114	TIN2	(Note 1)
P2 / 9	10	M2	115	TOUT2	(Note 1)
P2 / 8	11	M8	98	CLKOUT	(Note 1)
P2 / 7	12	M9	94	BERR	(Note 1)
P2 / 6	13	K13	74	BUSW	(Note 1)
P2 / 5	14	M10	90	BR	(Note 1)
P2 / 4	15	M12	87	BG	(Note 1)
P5 / 19	0	K2	123	RMC	(Note 1)
P5 / 18	1	K3	122	IAC	(Note 1)
P5 / 17	2	H12	71	DONE	(Note 1)
P5 / 16	3	G12	69	DREQ	(Note 1)
P5 / 15	4	H13	70	DACK	(Note 1)
P5 / 14	5	N3	110	IACK1	(Note 1)
P5 / 13	6	L5	109	IACK6	(Note 1)
P5 / 12	7	M5	108	IACK7	(Note 1)

Note 1: These signals are not required for inverse assembly. However, they may be useful for microprocessor analysis.

Table 3-1. Signal-to-Connector List (Continued)

E2414B Connector / Pin	Logic Analyzer Bit	Preprocessor Interface / PGA Pin	QFP Pin	Pin Mnemonic	Label
P5 / 11	8	L9	93	AVEC	(Note 1)
P5 / 10	9	J4	118	PB8	(Note 1)
P5 / 9	10	K4	119	PB9	(Note 1)
P5 / 8	11	N1	120	PB10	(Note 1)
P5 / 7	12	L2	121	PB11	(Note 1)
P5 / 6	13	G11	68	PA12	(Note 1)
P5 / 5	14	N12	91	HALT	(Note 1)
P5 / 4	15	L11	86	BCLR	(Note 1)
P6 / 19	0	D9	53	RXD2	(Note 1)
P6 / 18	1	E10	54	TXD2	(Note 1)
P6 / 17	2	C12	55	RCLK2	(Note 1)
P6 / 16	3	D11	56	TCLK2	(Note 1)
P6 / 15	4	B13	58	CTS2	(Note 1)
P6 / 14	5	C13	59	RTS2	(Note 1)
P6 / 13	6	E11	60	CD2	(Note 1)
P6 / 12	7	E12	61	SDS2	(Note 1)
P6 / 11	8	E13	63	RXD3	(Note 1)
P6 / 10	9	F11	64	TXD3	(Note 1)
P6 / 9	10	F12	65	RCLK3	(Note 1)
P6 / 8	11	F13	66	TCLK3	(Note 1)
P6 / 7	12	J13	73	DISCPU	(Note 1)
P6 / 6	13	H11	72	FRZ	(Note 1)
P6 / 5	14	N11	92	RESET	(Note 1)
P6 / 4	15	K5	117	WDOG	(Note 1)

Note 1: These signals are not required for inverse assembly. However, they may be useful for microprocessor analysis.

Table 3-1. Signal-to-Connector List (Continued)

E2414B Connector / Pin	Logic Analyzer Bit	Preprocessor Interface / PGA Pin	QFP Pin	Pin Mnemonic	Label
P1 / 3	CLK	M6	104	AS *	JCLOCK
P3 / 3	CLK	K9	85	DTACK	
P6 / 3	CLK	M8	98	CLKOUT	

* This pin must remain configured as AS for correct state analysis with the HP E2414B.

Servicing

The repair strategy for the HP E2414B is board replacement. However, table 3-2 lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales/Service Office for further information on servicing the board.

Table 3-2. Replaceable Parts

HP Part Number	Description
E2413-66502	Interface Circuit Board
E2414-66502	Personality Circuit Board
E2414-68704	Inverse Assembler Disk Pouch
E3408A	QFP Probe Adapter Assembly
1200-1679	Pin Protector

Dimensions

Figure 3-1 lists the dimensions for the HP E2414B circuit board. The dimensions are listed in inches and millimeters.

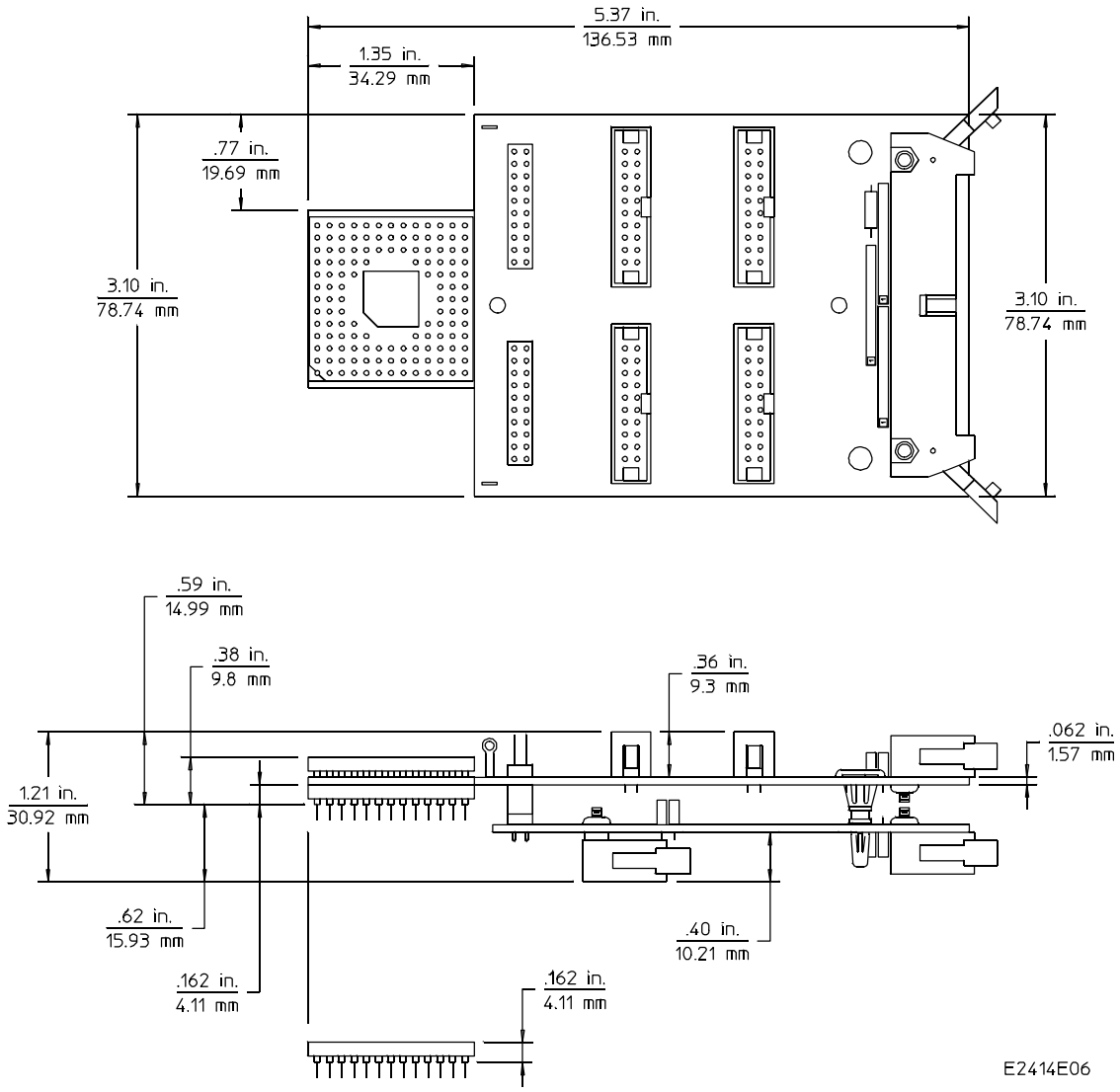

Figure 3-1. HP E2414B Dimensions

A

Troubleshooting

If you encounter difficulties while making measurements, use this section to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions. Error messages which may appear on the logic analyzer are listed below in quotes " ". Symptoms are listed without quotes.

If you are still having difficulties after trying the suggestions below, please contact your local Hewlett-Packard service center for additional assistance.

Target Board Will Not Bootup

If the target board will not bootup after connecting the preprocessor interface, the microprocessor or the preprocessor interface are not installed properly, or they are not making electrical contact.

- Verify that the microprocessor and the preprocessor interface are properly rotated and aligned.
- Verify that the microprocessor and the preprocessor interface are securely inserted into their respective sockets.
- Verify that the logic analyzer cables are in the proper sockets of the preprocessor interface and firmly inserted.
- Reduce the number of extender sockets (see also "Capacitive Loading").

"Slow or Missing Clock"

This error message might occur if the logic analyzer cards are not firmly seated in the HP 16500/16501 frame. Ensure that the cards are firmly seated.

This error might also occur if the target system is not running properly. Ensure that the target system is on and operating properly.

If the error message persists, check the that the logic analyzer pods are connected to the proper connectors, as listed in table 1-1.

For HP 1650A and HP 16510A Logic Analyzers, check the preprocessor interface power fuse in the logic analyzer.

"No Configuration File Loaded"

Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500 disk operation menu. Selecting Load {All} will cause incorrect operation when loading most preprocessor interface configuration files.

"Selected File is Incompatible"

The logic analyzer displays this message if you try to load a configuration file for the wrong module. Ensure that you are loading an appropriate configuration file for your logic analyzer.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

No Inverse Assembly

Verify that the inverse assembler has been synchronized by placing an opcode at the top of the display and pressing the Invasm key (see "Inverse Assembler" in Chapter 2).

Incorrect Inverse Assembly

This problem is usually caused by a hardware problem in the target system. A locked status line will often cause incorrect or incomplete inverse assembly.

- Check the activity indicators for status lines locked in a high or low state.
- Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values. These labels must remain as they are configured by the configuration file.
- Verify that all microprocessor caches and memory managers have been disabled. In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly, but it may be incorrect since some of the execution trace was not visible to the logic analyzer.
- Verify that storage qualification has not excluded storage of all the needed opcodes and operands.

No Activity on Activity Indicators

On the HP 1650A, HP 1651A, and HP 16510A Logic Analyzers, if there is no activity the fuse which allows power to the preprocessor interface is probably blown. Check the fuse in the logic analyzer. On the other logic analyzers, if there is no activity, one of the cables, board connections, or preprocessor interface connections is probably loose. Check all connections.

Capacitive Loading

Excessive capacitive loading can cause signals to degrade, resulting in incorrect capture by the preprocessor interface or system lockup in the microprocessor. All preprocessor interfaces add additional capacitive loading. The following techniques will reduce the capacitive loading:

- Remove as many pin protectors, extenders, and adapters as possible.
- If a passive preprocessor interface is available, try using that instead of an active one.

"State Clock Violates Overdrive Specification"

At least one 16-channel pod in the state analysis measurement stored a different number of states before trigger than the other pods. This is usually caused by sending a clocking signal to the state analyzer that does not meet all of the specified conditions, such as minimum period, minimum pulse width, or minimum amplitude. Poor pulse shaping could also cause this problem.

Note 

The error message "State Clock Violates Overdrive Specification" should only occur for HP 1650A,B, HP 1652B, HP 16510A,B, and HP 16511B Logic Analyzers with the Clock Period field set to < 60 ns. If this error message is observed with the Clock Period set to > 60 ns, you may have a faulty logic analyzer. If a failure is suspected in your logic analyzer, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the instrument.

Unwanted Triggers

Unwanted triggers can be caused by unexecuted prefetches. Add the prefetch queue depth to the trigger address to avoid this problem.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern did not occur. Verify that the triggering pattern is correctly set.

If a "don't care" trigger condition is set, this message indicates:

- For an HP 16511B Logic Analyzer, only one of the two cards is receiving its state clock. Refer to "Slow or Missing Clock."
- For an HP 1650A,B, HP 1652B, or HP 16510A,B Logic Analyzer, the pattern duration is probably set to less than (<) instead of greater than (>). Since a "don't care" pattern is always true, the "less than" condition is never satisfied. Set the trace menu correctly for the measurement that is desired.

Intermittent Data Errors

This problem is usually caused by incorrect signal levels. Adjust the threshold level of the data pod. Use an oscilloscope to check the signal integrity of the data lines, as needed.

Bent Pins

Bent pins on the preprocessor interface, pin protectors, or adapters can cause system errors or inverse assembly errors. Ensure all pins are properly aligned and making contact.

"Time from Arm Greater Than 41.93 ms."

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

No Setup/Hold Field on Format Screen

The HP 16540/16541A,D or HP 16542A Logic Analyzer cards are not calibrated. Refer to your logic analyzer reference manual for procedures to calibrate the cards.

"Default Calibration Factors Loaded" (16540/41/42)

The default calibration file for the logic analyzer was loaded. The logic analyzer must be calibrated when using HP 16540A,D, HP 16541A,D or HP 16542A cards. Refer to your logic analyzer manual for procedures to calibrate the master clocking system, and ensure that the "cal factors" file is saved.